(19) Europäisches Patentamt
European Patent Offic
Offic européen d s brev ts

(11) Publication number : **0 506 473 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **92302735.3**

(51) Int. Cl.[5] : **H01L 21/76,** H01L 21/316

(22) Date of filing : **27.03.92**

(30) Priority : **28.03.91 US 677649**

(43) Date of publication of application :
30.09.92 Bulletin 92/40

(84) Designated Contracting States :
DE FR GB IT

(71) Applicant : **SGS-THOMSON MICROELECTRONICS, INC.**
1310 Electronics Drive
Carrollton Texas 75006 (US)

(72) Inventor : **Miller, Robert Otis**
5523 Vaden Street, The Colony
Denton, Texas 75076 (US)

(74) Representative : **Palmer, Roger et al**
PAGE, WHITE & FARRER 54 Doughty Street
London WC1N 2LS (GB)

(54) Method of producing isoplanar isolated active regions.

(57) A method is provided for forming isoplanar isolated regions in an integrated circuit, and an integrated circuit formed according to the same. According to a first disclosed embodiment, a first epitaxial layer is formed over a substrate, the substrate having a (100) crystal orientation. A first masking layer is formed over the first epitaxial layer. The first masking layer is patterned and the first epitaxial layer is etched to form openings. The sidewalls of these openings have a (111) crystal orientation. The first masking layer is then removed and a second masking layer is formed in the openings. The first epitaxial layer is anodized and oxidized. The second masking layer is removed and a second epitaxial layer is formed in the openings. According to an alternate embodiment, after the first epitaxial layer is anodized, the second epitaxial layer is formed in the openings and the first epitaxial layer is then oxidized. According to a further alternate embodiment, the first epitaxial layer is anodized and oxidized after the second epitaxial layer is formed in the openings.

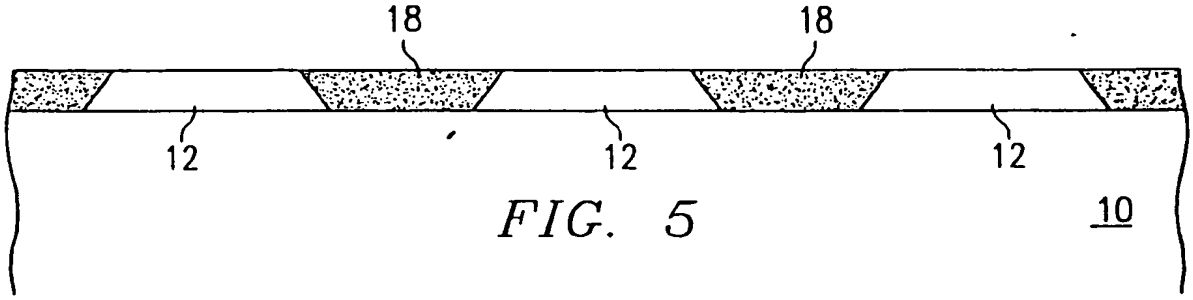

FIG. 5

EP 0 506 473 A2

The present invention relates generally to semiconductor integrated circuit processing, and more specifically to producing isoplanar isolated active regions.

The trend to continue to miniaturize semiconductor integrated circuits to achieve submicron feature sizes and increase the number of devices fabricated on the integrated circuit has required faster downscaling of lateral dimension than vertical dimensions, resulting in larger aspect ratios in surface topography. With densely packed circuits, there is a need to isolate components which are adjacent to each other to prevent leakage current. As with MOS transistors, current flows along the surface between the source and drain. The MOS transistors formed adjacent to each other must be separated by an isolation film thick enough so that there is no field induced currents flowing under the film. Isolating adjacent components in such a manner as to minimize surface topography is known as isoplanar isolation.

Before the introduction of local oxidation of silicon (LOCOS) processes, it was common to provide MOS fi ld isolation by growing a thick layer of field oxide across the wafer, then masking and removing oxide where active areas were to be formed. Using a wet etch step, this process did not allow for the creation of vertical oxide sidewalls. However, potential step coverage problems were avoided with this process, but at the expense of layout space, thus limiting device performance.

The introduction of LOCOS was a great technological improvement. However, several problems occurred with LOCOS. Non-uniform thermal oxidation of a wafer surface, in the original LOCOS form, always incurred lateral encroachment, or tapering of th field oxide in the active areas growing under a nitrid mask. This tapering effect, called "birdbeaking" is a sacrifice of active areas that becomes significant for feature sizes less than 1.5 microns. Attempts to suppress birdbeaking caused stress-related defects in the nearby substrate. Process complexity then occurred in attempting to avoid these stress-related defects.

To achieve submicron geometries, there can be little or no physical loss of the active areas as occurs with the birdbeaking phenomenon. Thus, it is necessary to reconsider the prior art approach where vertical walls are needed to manufacture devices with feature sizes less than 1.5 microns. Abrupt topography results from vertical walls, causing difficulty in subsequent patterning and etching of films deposited over the wafer. Moreover, vertical walls, or near vertical walls, can only be achieved by dry etching of oxide. Damage to the active areas may result from marginal overetching.

For a number of years, various observers have noticed the potential value of selective epitaxial refill of contact holes etched through field oxide in order to achieve a completely planar surface. Selective epitaxial refillr may cause defects near the active area/field oxide interface because the epitaxial layer is unable to grow in the (111) direction. Anomalies in epitaxial growth may also result due to any etching damage of the starting surface before the epitaxial refill.

It would be desirable for a semiconductor process to produce isoplanar isolated active and field regions.

It is a further object of this invention to provide such a semiconductor fabrication process by anodizing and oxidizing the field oxide regions and refilling the remaining areas with epitaxial silicon.

It is yet another object of this invention to provide such a semiconductor fabrication process for making isoplanar active regions separated by isoplanar field oxide isolated regions which are suitable for use with small device geometries.

Other objects and advantages of this invention will be apparent to those of ordinary skill in the art having reference to the following specification, together with its drawings.

The invention may be incorporated into a method for forming an integrated circuit, and the integrated circuit formed thereby, by producing isoplanar isolated regions on the surface of a wafer having a (100) crystal orientation. A first epitaxial layer is formed over the substrate and then patterned and etched to form openings in the layer. This first epitaxial layer is anodized and oxidized. A second epitaxial layer is then formed in the openings. The second epitaxial layer may be formed after the first layer is anodized but before the first layer is oxidized. The second epitaxial layer may also be formed before the first layer is anodized and oxidized.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figures 1-5 are cross-sectional views of the fabrication of an integrated circuit, at various steps, according to one embodiment of the invention.

Figures 6-10 are cross-sectional views of the fabrication of an integrated circuit, at various steps, according to an alternative embodiment of the invention.

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fab-

rication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Referring to **Figur 1**, an integrated circuit is to be formed on a silicon substrate **10**. The substrate must be a wafer which has a single crystal structure with the proper crystal orientation. The planes of the specific orientation are known in the art as the Miller indices, identified by a series of three numbers. The two most common crystal orientations for a silicon wafer are the (100) and (111) planes. In this invention, the substrate should preferably be from a wafer having the (100) orientation. The substrate may be doped with a p-type dopant as known in the art to act as an etch stop during subsequent anisotropic etch processes.

A first epitaxial layer of silicon **12** is then grown on the substrate **10** as known in the art. The epitaxial layer will conform to the same (100) crystal orientation as that of the underlying substrate. The epitaxial layer may be doped with an n-type dopant as known in the art to improve its etching properties. A first masking layer **14** is then deposited on the first epitaxial layer **12** as known in the art. The first masking layer is preferably silicon dioxide (SiO_2) or silicon nitride (Si_3N_4).

Referring to **Figure 2**, the integrated circuit is then patterned to form openings in the first masking layer. The first epitaxial layer **12** is etched to form openings in the layer as shown in **Figure 3**. The etch process is preferably an anisotropic etch which results in the sidewalls of the first epitaxial layer having a (111) crystal orientation or a nearly 54.74 degree slope. Among the alternative anisotropic etchants that may be used for this process depending upon the masking layer used may include ethylene diamine, pyrocatechol ("EDP"), sodium hydroxide ("NaOH"), potassium hydroxide ("KOH") or hydrazine ("N_2H_4"). The first masking layer **14** is then removed by known methods.

An alternative etch process consists of a wet/dry etch combination as known in the art to produce the same (111) crystal orientation. Because the wet/dry etch process may result in defects in the crystal orientation of the sidewalls of the first epitaxial layer **12**, passivation of the layer, such as a boron implant, may be required to eliminate such defects.

Referring to **Figure 4**, a second masking layer **16** is deposited across the wafer surface and then patterned in the openings between the isolated first epitaxial layer **12** regions. The patterning of layer 16 involves a non-critical photolithographic alignment. This second masking layer 16 is preferably Si_3N_4. A thin layer of approximately 100-200 Angstroms of oxide may be grown or deposited under layer 16 before layer 16 is deposited to protect the underlying first epitaxial layer 12 and the substrate 10 during deposition and subsequent removal of layer 16. The first epitaxial layer **12** is then anodized converting the n-type doped layer to porous silicon. The n-type doped epitaxial layer will anodize faster than the p-type doped substrate. Layer **12** is subsequently oxidized to form isolated regions of oxide having sidewall angles of 54.73 degrees or the (111) crystal orientation.

Anodization of the isolated regions of layer **12** before oxidation allows layer **12** to retain its same volumetric size. The oxide expands to fill substantially the original space occupied by the anodized epitaxial silicon, thus creating little or no deformation of the integrated circuit. This anodization process of converting silicon to dioxide, known in the art, is described more filly in United States Patent No. 4,628,591, Serial No. 666,698, issued December 16, 1986, Method For Obtaining Full Oxide Isolation Of Epitaxial Islands In Silicon Utilizing Selective Oxidation Of Porous silicon, of E.S. Zorinsky and D.B. Spratt. The second masking layer **16**, used as an anodization mask, is subsequently removed.

Referring to **Figure 5**, a second layer of epitaxial silicon **18** is then grown in the active regions between the isolated regions of the first epitaxial layer **12**. The regions of epitaxial layer **18** are now suitable for fabrication of MOS devices isolated by the epitaxial regions **12**.

An alternative embodiment includes growing and etching the first epitaxial layer **12** as above, again preferably having been doped with an n-type dopant. The second masking layer **16** is deposited. After layer 12 is anodized, the second masking layer 16 is removed. The second epitaxial layer **18** is then grown between the remaining isolated regions of the first epitaxial layer **12**. Layer **12** is then oxidized to form insulating regions around layer **18** as shown in **Figure 5**. A further alternative embodiment to the above process includes growing and etching the first epitaxial layer **12** as above. The second masking layer 16 is not deposited. The second epitaxial layer **18** is grown in between the isolated regions of layer **12**. Layer **12** is subsequently anodized and oxidized to form the insulating regions around the epitaxial regions **18** as shown in **Figure 5**. Because the isolated regions of layer **12** are doped with an n-type dopant, these regions will anodize at a faster rate than the second epitaxial layer **18** used to refill the active regions between the regions of layer **12**.

Referring to **Figure 6**, an additional alternative method is shown. The process steps are the same as above to grow a first epitaxial layer **32** over a substrate **30**, deposit and pattern a first masking layer **34** and etch layer **32**. The crystal orientations are the same as those described above. Again, epitaxial layer **32** may be doped with an n-type dopant to improve its etching and anodizing properties.

Next, a second masking layer **36** is conformally formed over the first masking layer **34**. This second masking layer **36** is preferably silicon nitride or silicon nitride over a thin layer of oxide. The oxide may be grown or deposited while the silicon nitride is depo-

sited by methods known in the art. If a thin layer of oxide is first formed under the silicon nitride, it generally will have a thickness between 100 and 200 Angstroms. A polymer layer **38** is then non-conformally spun onto the surface of the wafer. Layer **38** may be typically a polyimide or photoresist.

Referring to **Figure 7**, the second masking layer **36** and polymer layer **38** are then etched, preferably by a plasma etch. One of the advantages of this process is that the etch step, after layer **38** is spun onto the wafer, becomes self-aligning. Referring to **Figure 8**, the first masking layer 34 is removed. The first epitaxial layer **32** is then anodized.

Referring to **Figure 9**, the polymer layer **38** is preferably removed after anodization but before oxidation of layer **32**. Layer **32** is then oxidized. The second masking layer **36** is removed. At this stage of the process, there are isolated regions of oxide formed from the first epitaxial layer **32**. Referring to **Figure 10**, a second epitaxial layer **40** is grown in the active regions between the isolated regions of oxide. These regions of layer **40** are now suitable for fabrication of MOS devices isolated by the epitaxial regions **32**. This process may also be used for any device which needs to be isolated laterally by oxide. For example, thick pitaxial layers may make this process suitable for use in manufacturing high-voltage semiconductor devices.

Growth of the two epitaxial layers **12** and **18** as shown in **Figure 5** and layers **32** and **40** as shown in **Figure 10**, forms a planar surface for subsequent processes. Anodizing and oxidizing epitaxial silicon forms isoplanar insulating regions of oxide around the active areas. The epitaxial silicon growth or epitaxial refill between the insulating regions of oxide provides for isolated active regions for fabrication of devices without sacrificing device performance or usable layout space.

Claims

1. A method of producing isoplanar isolated regions in an integrated circuit comprising the steps of:
   (a) forming a first epitaxial layer over a substrate;
   (b) patterning the first epitaxial layer to form isolated regions;
   (c) forming a second epitaxial layer in between the isolated regions; and
   (d) oxidizing the first epitaxial layer.

2. A method of producing isoplanar isolated regions in an integrated circuit comprising the steps of:
   forming a first epitaxial layer over a substrate;
   forming a first masking layer over the first epitaxial layer;
   patterning the first masking layer;
   etching the first epitaxial layer;
   forming a second masking layer in the openings;
   anodizing the first epitaxial layer;
   oxidizing the first epitaxial layer;
   removing the second masking layer; and,
   forming a second epitaxial layer in the openings.

3. A method as claimed in claim 1 wherein step (d) is performed before step (c).

4. A method of producing isoplanar isolated regions in an integrated circuit comprising the steps of:
   forming a first epitaxial layer over a substrate;
   forming a first masking layer over the first epitaxial layer;
   patterning the first masking layer;
   etching the first epitaxial layer;
   forming a polymer layer over the surface of the wafer;
   etching the polymer;
   removing the first masking layer;
   anodizing the first epitaxial layer;
   oxidizing the first epitaxial layer; and
   forming a second epitaxial layer in the openings.

5. An integrated circuit, comprising:
   a substrate; and,
   epitaxial regions disposed over the substrate separated by oxide regions wherein the epitaxial regions having an inverted trapezoidal volume are wider at the top than at the bottom.

6. The method of any one of claims 1, 2, 3 or 4, wherein a p-type dopant has been implanted into the substrate.

7. The method of any one of claims 1, 2, 3 or 4, wherein the first epitaxial layer is doped with an n-type dopant.

8. The method of claim 1, wherein the first epitaxial layer is anodized before the second epitaxial layer is formed.

9. The method of claim 1, wherein the first epitaxial layer is anodized after the second epitaxial layer is formed.

10. The method of claim 2, wherein the first masking layer is remov d after the first epitaxial layer is etched.

11. The method of claim 2, wherein the first masking

layer is removed after the first epitaxial layer is anodized.

12. The method of claim 2 or 4, wherein the first masking layer is either silicon dioxide (SiO_2) or silicon nitride (Si_3N_4).

13. The method of claim 8, wherein a second masking layer is deposited before anodization of the first epitaxial layer and removed after anodization of the first epitaxial layer.

14. The method of claim 4, wherein a second masking layer is formed before the polymer layer is formed.

15. The method of claim 2 or 4, wherein the second masking layer is nitride (Si_3N_4) or a layer of silicon nitride (Si_3N_4) over a layer of oxide.

16. The method of claim 1, 2 or 3 or the integrated circuit of claim 5, wherein the crystal orientation of the substrate is the (100) plane.

17. The integrated circuit of claim 15, wherein the sidewalls of the epitaxial regions have the crystal orientation of the (111) plane.

18. The method of claim 16, wherein the etching step of claim 2 or the patterning step of claim 1 or 3 creates sidewalls having the crystal orientation of the (111) plane.

19. The method of claim 15, wherein the etching or patterning step is an anisotropic etch, preferably a combination wet/dry etch, which produces sidewalls having a (111) crystal orientation.

20. The method of claim 19, wherein the anisotropic etchant is EDP.

21. The method of claim 19 or 20, further comprising the step of passivating the sidewalls, preferably using a boron implant.

22. The method of claim 4, wherein the polymer layer is removed after anodizing the first epitaxial layer.

23. The method of claim 14, wherein the polymer layer is removed before anodizing the first epitaxial layer if the second masking layer is formed.

24. The method of claim 14, wherein the polymer layer is removed after anodizing the first epitaxial layer if the second masking layer is formed.

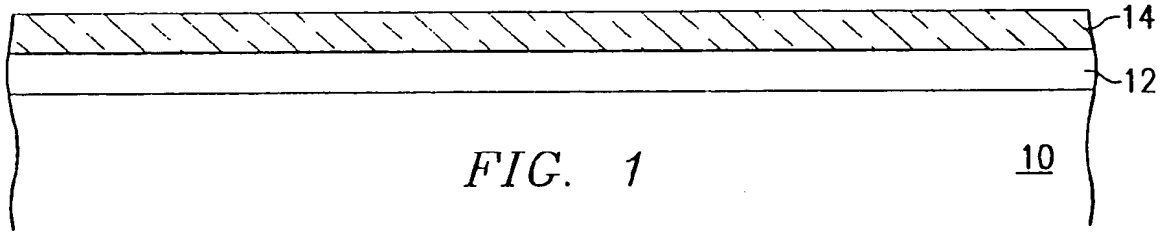

FIG. 1

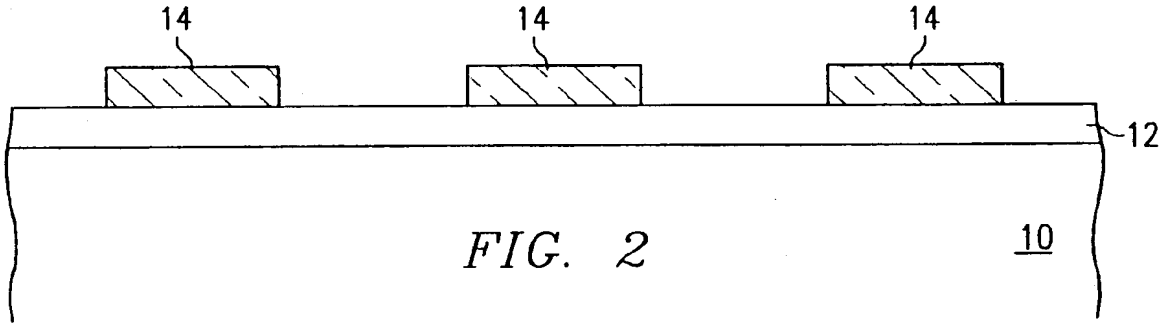

FIG. 2

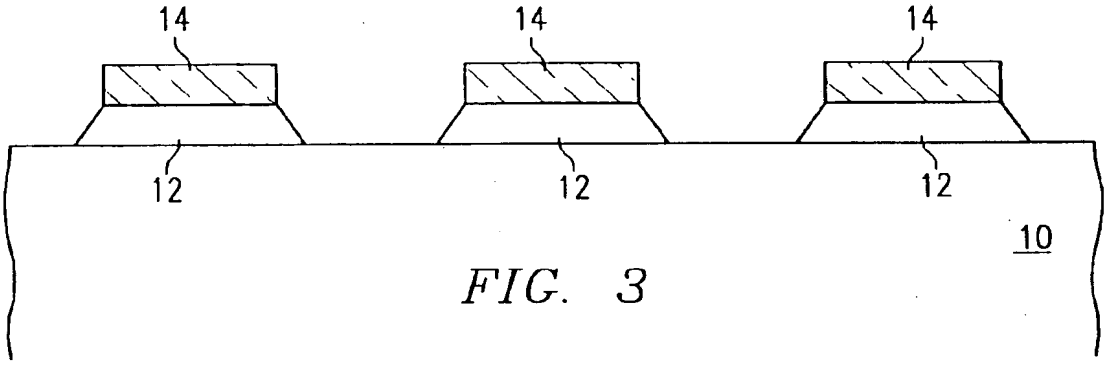

FIG. 3

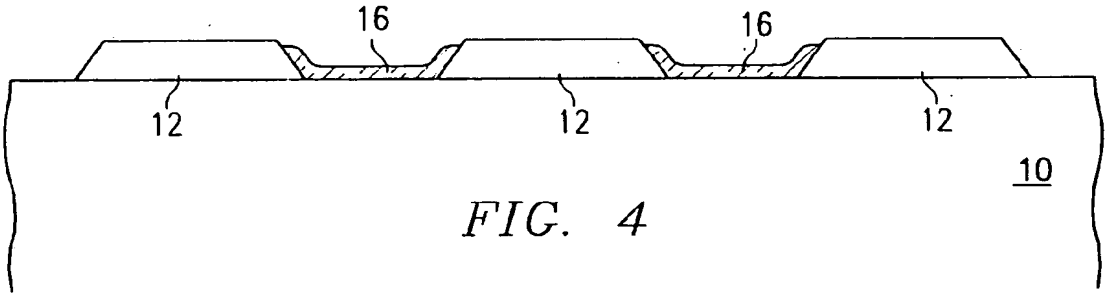

FIG. 4

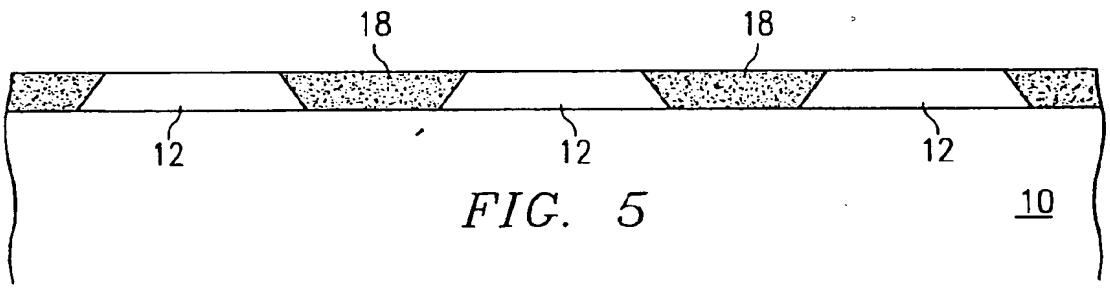

FIG. 5

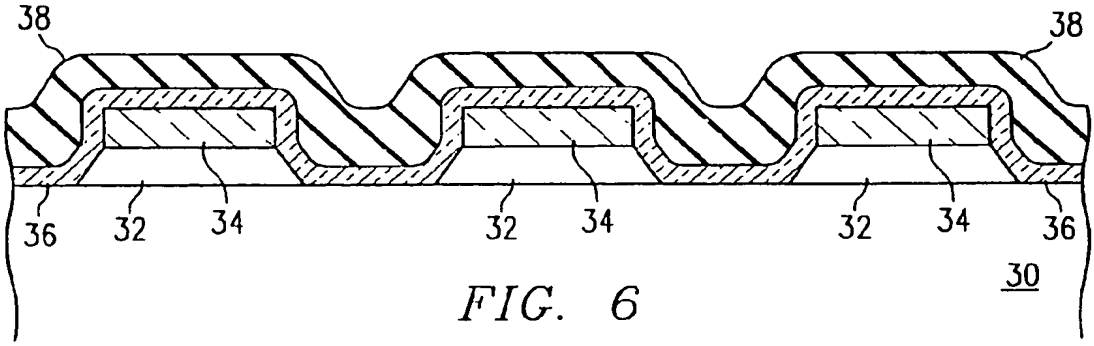

FIG. 6

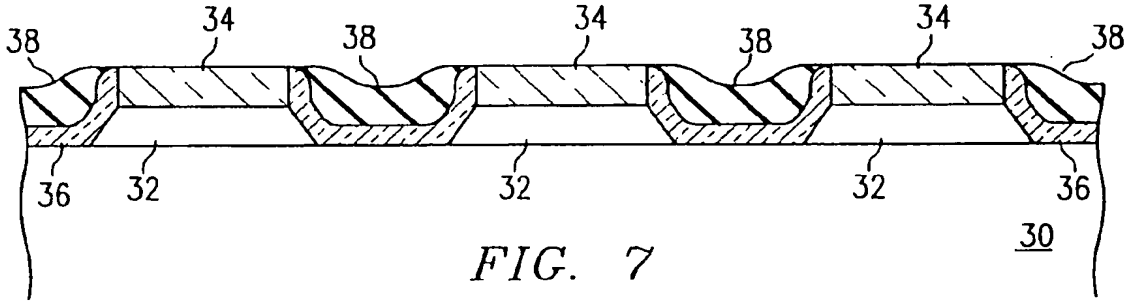

FIG. 7

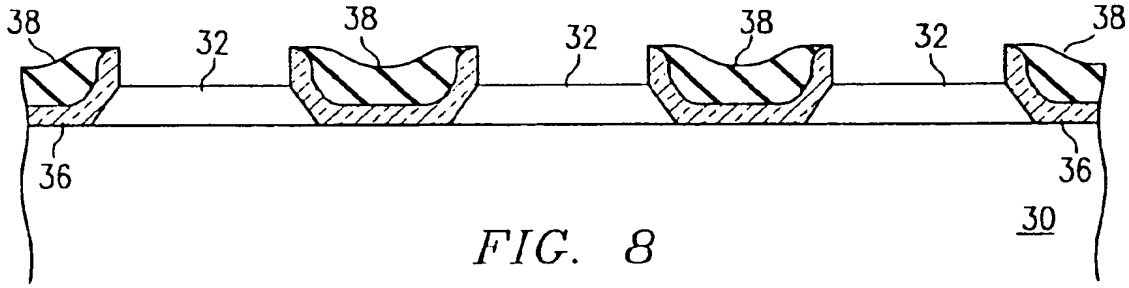

FIG. 8

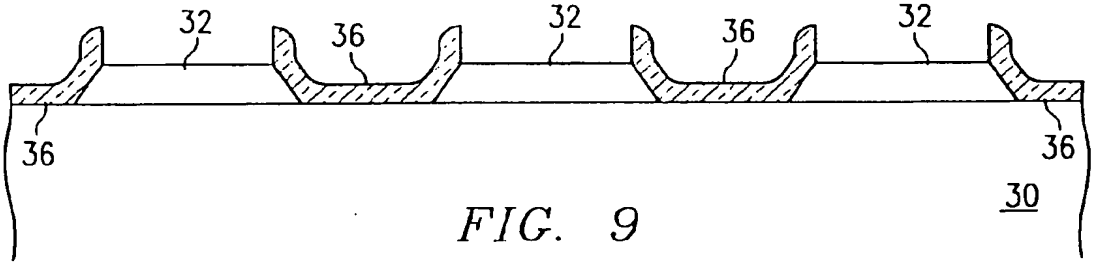

FIG. 9

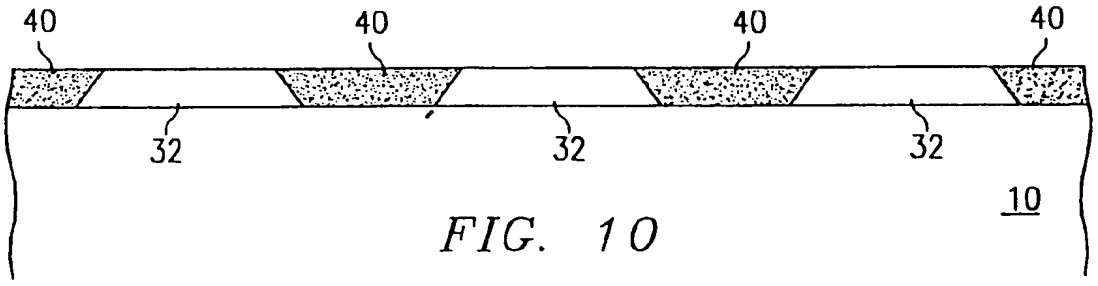

FIG. 10

(19) Europäisches Patentamt
European Patent Offic
Office uropé n d s brevets

(11) Publication number : **0 506 473 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **92302735.3**

(51) Int. Cl.[5] : **H01L 21/76,** H01L 21/316

(22) Date of filing : **27.03.92**

(30) Priority : **28.03.91 US 677649**

(43) Date of publication of application :
30.09.92 Bulletin 92/40

(84) Designated Contracting States :
DE FR GB IT

(88) Date of deferred publication of search report :
13.09.95 Bulletin 95/37

(71) Applicant : **SGS-THOMSON MICROELECTRONICS, INC.**
1310 Electronics Drive
Carrollton Texas 75006 (US)

(72) Inventor : **Miller, Robert Otis**
5523 Vaden Street,
The Colony
Denton, Texas 75076 (US)

(74) Representative : **Palmer, Roger et al**
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(54) Method of producing isoplanar isolated active regions.

(57) A method is provided for forming isoplanar isolated regions in an integrated circuit, and an integrated circuit formed according to the same. According to a first disclosed embodiment, a first epitaxial layer is formed over a substrate, the substrate having a (100) crystal orientation. A first masking layer is formed over the first epitaxial layer. The first masking layer is patterned and the first epitaxial layer is etched to form openings. The sidewalls of these openings have a (111) crystal orientation. The first masking layer is then removed and a second masking layer is formed in the openings. The first epitaxial layer is anodized and oxidized. The second masking layer is removed and a second epitaxial layer is formed in the openings. According to an alternate embodiment, after the first epitaxial layer is anodized, the second epitaxial layer is formed in the openings and the first epitaxial layer is then oxidized. According to a further alternate embodiment, the first epitaxial layer is anodized and oxidized after the second epitaxial layer is formed in the openings.

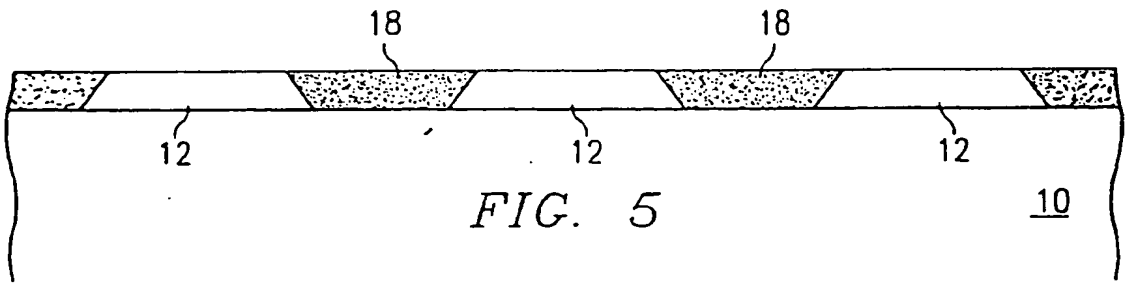

FIG. 5

EP 0 506 473 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 30 2735

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 222 225 (IBM) * column 2, line 35 - column 4, line 20; figures 1,2 *	1,3,5	H01L21/76 H01L21/316
A	US-A-4 975 759 (DELCO ELECTRONICS CORP.) * column 3, line 9 - column 4, line 3 *	1,5,17	
A	FR-A-2 189 871 (IBM) * figure 1 *	1	
A,D	US-A-4 628 591 (TEXAS INSTRUMENTS INC.) * figures 4-6 *	3,4	
A	PATENT ABSTRACTS OF JAPAN vol. 6 no. 132 (E-119) [1010] ,17 July 1982 & JP-A-57 056942 (TADATSUGU ITOU) 5 April 1982, * abstract *	3,4	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 July 1995	Vancraeynest, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)